A wideband analog correlator system for AMiBA

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ABSTRACT

A wideband correlator system with a bandwidth of 16 GHz or more is required for Array for Microwave Background Anisotropy (AMiBA) to achieve the sensitivity of $10\,\mu$K in one hour of observation. Double-balanced diode mixers were used as multipliers in 4-lag correlator modules. Several wideband modules were developed for IF signal distribution between receivers and correlators. Correlator outputs were amplified, and digitized by voltage-to-frequency converters. Data acquisition circuits were designed using field programmable gate arrays (FPGA). Subsequent data transfer and control software were based on the configuration for Australia Telescope Compact Array. Transform matrix method will be adopted during calibration to take into account the phase and amplitude variations of analog devices across the passband.

Keywords: Wideband correlator, voltage-to-frequency converter, AMiBA

1. INTRODUCTION

The Array for Microwave Background Anisotropy[1] (AMiBA) is a ground-based millimeter-wave interferometric array, designed to study the anisotropy of Cosmic Microwave Background (CMB), and to search for high red-shift clusters by observing the Sunyaev-Zel'dovich Effect (SZE). The final array will have 13 120-cm reflectors and receivers mounted on a 6-meter diameter platform to achieve a two arc-minute resolution. The dual-polarization receivers use cryogenically cooled, low-noise amplifiers, operating in the 85-104 GHz band, with a system noise temperature of 150K. This band was chosen to minimize the foreground synchrotron radiation. The RF signals are down-converted with sub-harmonically pumped mixers to the 2-18 GHz IF band. After distribution, the IF signals from each pair of antennas are multiplied in the correlator.

The spatial variations in the cosmic microwave background are of the order of several tens of μK. To achieve this level of sensitivity, with system temperatures around 50K, correlators with bandwidths of several GHz are required. Nowadays digital correlators with moderate bandwidths of several hundred MHz are widely used in spectral line observations. Digital correlators[2] have the advantage of being easily re-configured for different bandwidths and resolutions. However very wide band digital correlators require high-speed sampling, and suffer from sensitivity degradation due to the coarse quantization steps usually employed in the samplers. On the other hand, analog correlators with wideband microwave components can provide wider bandwidths and higher efficiency. In the analog case, regular calibration is required to measure the non-ideal behavior of each component.

The AMiBA correlator requires a modest amount of frequency resolution, in order to distinguish the CMB signals from the galactic foreground emission[3] and to overcome bandwidth smearing[4] effects in the interferometer. It uses very wideband analog multiplier elements arranged as a lag correlator. This device measures the degree of correlation of pairs of input signals at a series of delays. The resulting correlation function is then Fourier transformed to give the cross power spectrum. The range of delay over which the correlation function is measured determines the frequency resolution.

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2. ARCHITECTURE

For the 13-element system, there are a total of 325 = (13*12/2)*4 + 13 correlations between two polarization outputs of each receiver. The network to distribute 2-18 GHz IF signals from receivers to correlators is implemented by cascading three sections. In the first 2 sections, IF amplifiers (CELERITEK) with gain of 30 dB and P1dB of 20 dBm, in conjunction with 4-way power dividers (MERRIMAC), provide power amplification and division.

In the 1st section, -10 dB directional couplers draw part of the IF signals into power detectors for monitoring receiver gain variation. 18-GHz low-pass filters (K&L) are used to define the upper limit of the passband to avoid aliasing. Slope equalizers (INMET) compensate for gain slopes occurring in the following modules to optimize the effective bandwidth, which plays an important role in determining the overall sensitivity. Immediately after the 1st section, one of 4 IF output signals is fed into an additional (XY) module to measure the correlation between the 2 polarizations from one receiver.

In the 2nd section, there are 2-way switches, which allow one of the correlator inputs in the 3rd section to be connected to either right-circular (R) or left-circular (L) polarization. Thereby, the number of correlator modules required is reduced by one half. One of 2 sets of correlations – (RR, LL), and (RL, LR) – can be measured alternately.

In the 3rd section, as shown in Fig. 1, 4 x 4 correlator modules are stacked in a metallic frame as a basic block. Horizontal 4-way power dividers are used to provide IF signals to correlator inputs on one side of the block via BMA blind mate connectors, while vertical 4-way power dividers feed the other side. For the 13-element system, the final design will use 2 electronic cabinets, each containing 2 x 3 correlator blocks.

The lag correlator module (Marki Microwave) produces cross correlations of two inputs at 4 different delays. The delay increment of 25 pico-seconds sets the upper frequency limit of the IF to 20 GHz, according to the sampling theorem. The multipliers are double balanced mixers, used in a local oscillator starved mode. The following low-noise feedback operational amplifier (OPA) circuits provide low-frequency voltage amplification with a low-pass 3-dB cut-off frequency around 10 KHz. Due to the high output impedance of the low-level-pumped mixers (~ 100 K ohm), OPAs (e.g. OPA637) with low current noise were used to minimize the backend noise contributions.

Analog-to-digital conversion and integration is achieved with a voltage-to-frequency converter / counter scheme. Oscillators within each back-end processing integrated circuit (the readout chip) generate square waves with frequencies modulated by the input voltages. Accumulation occurs in the following 24-bit up/down counters. During accumulation, the direction of counting is controlled by the DIR signal to demodulate the phase switching performed up-stream in the receivers. The results of counters are copied to scan-out registers during a short DUMP period between two integrations. The counters are reset shortly after DUMP. Data in the scan-out registers are shifted out in series, and then accommodated by shift registers in the data acquisition circuit during the SCAN period. After the SCAN is complete, the correlator control computer (CCC) begins the direct memory access (DMA) process to retrieve the data.

The data acquisition circuit is implemented with a programmable gate array (Xilinx FPGA Spartan IIE). In response to event signals from CCC, the circuit is able to act as a memory buffer between readout chips and CCC, to generate control signals for readout chips, as well as phase switching signals for the receivers.

The Walsh functions with up to 64 state changes in a cycle are used to implement the phase switching. Due to the low flicker noise corner frequency of the correlator modules, a slow phase switching suffices. A complete 64-state cycle takes 0.05s. In the current design, limited by number of I/O connectors of the programmable gate arrays that we used, additional circuitry is needed to generate a total of 176 demodulation signals for the 13-element system,.

The correlator control computer was an industrial computer, with Red Hat Linux as the operating system. 3 special-purpose interface cards provided by Australia Telescope National Facility (ATNF) were installed – a correlator PCI interface card, an Australia Telescope Distributed Clock (ATDC), and an Event Generator. The correlator PCI interface functions as a block of memory to allow the connection between the PCI bus and the data acquisition circuit. The ATDC is used as the central time keeper for the array. An 8-MHz clock from ATDC synchronizes all the digital processes. The Event Generator sends out timed interrupts for the system.
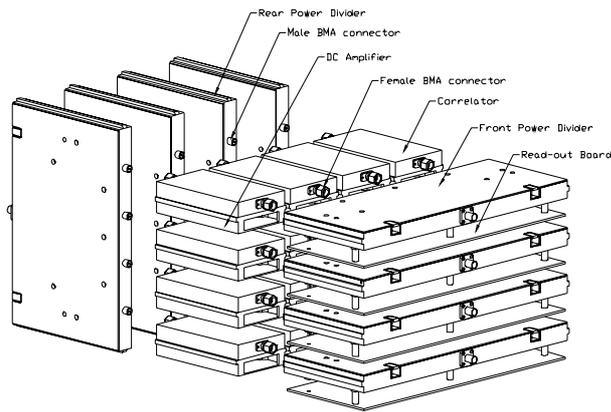
Fig. 1. In the 3rd section, each correlator block has 4 x 4 correlator modules, fed by horizontal and vertical power dividers.
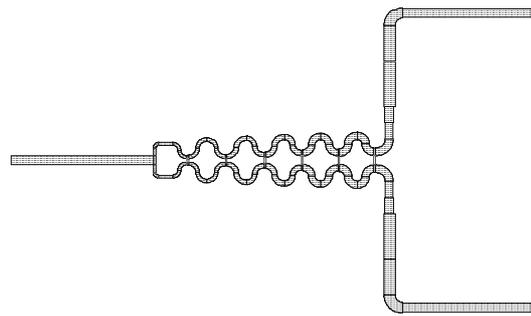
Fig. 2. Layout of the 2-way power divider, used as one stage of the 4-way power divider.
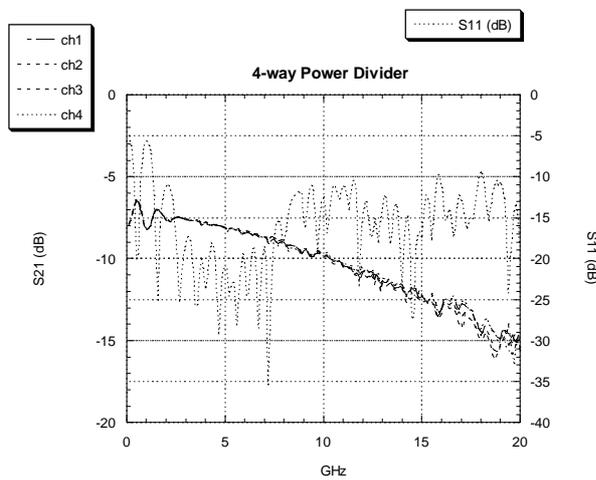
Fig. 3. Transmission and reflection of a custom 4-way power divider.
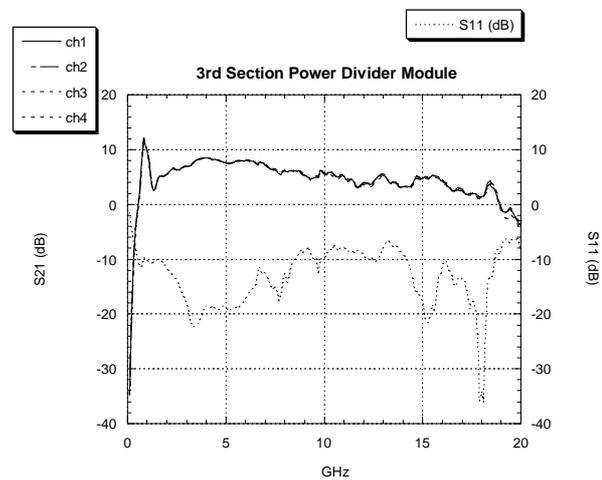
Fig. 4. Transmission and reflection of a 3rd section power divider module.

3. FOUR-WAY POWER DIVIDER MODULE

To accommodate the large spacing between correlator module inputs in the correlator block, 4-way power divider modules for the front and the rear sides, were designed. Two stages of MMIC IF amplifiers (Triquint TGA8300) were cascaded in front of the power dividers to provide an additional gain of 14 dB. Using Cu-clad substrates (12-mil thick Arlon 25N) with embedded resistive layers (100 Ohm/square Ohmega-ply) under top metal layers, planar resistors used in Wilkinson power dividers can be implemented by defining the proper footprints and removing the metal above. Thereby, the parasitic capacitance that comes with soldered chip resistors is avoided. As shown in Fig. 2, microstrip radial bends were widely used in the layout to minimize the inter-coupling between parallel transmission lines. The cavity resonance is removed by using metallic irises suspended from the cover to confine the circuits within narrow channels. In Fig.3, the measured return loss is better than 10 dB from 2 to 20 GHz. However, the transmission showed a significant amount of loss (about 1.7 dB at 2 GHz, and 8.3 dB at 18 GHz, with a slope of 6.6 dB), additional to the ideal 6 dB 4-way division loss. From the software simulation and measurements with transmission lines of different lengths,

the cause was identified to be the shunt resistive strips underneath the top metal of microstrip lines. Estimated loss is about 0.04 dB /mm at 20 GHz. In theory[5], 7-section power dividers are required to meet the reflection and isolation requirements over the 10:1 bandwidth. However, the rather long transmission lines between two stages can be designed as multi-section quarter-wavelength transformers to optimize the performance of power dividers with 6 sections. The transmission and reflection of an assembled module is shown in Fig. 4.

4. CORRELATOR MODULE

The core of the correlator system is the lag correlator module. Within each module, two stages of 2-way power dividers were cascaded to split the IF signals to 4 multipliers. Each multiplier is placed at different distances from two corresponding power divider outputs. The delay differences between 2 signal paths (from module inputs to multiplier inputs) were specified to be +37.5, +12.5, -12.5, and –37.5 pico-seconds, respectively. The output voltages from 4 lags can be transformed to be 2 complex frequency points in the cross power spectrum. Double-balanced mixers[6] were used as the multipliers with low power inputs. The low-barrier Silicon Schottky diode ring quads (Microsemi) were mounted between two ultra-wideband baluns. To avoid the reflection due to the discontinuity, the entire circuit, including 4-way power dividers and baluns, were fabricated on a single microwave substrate.

Due to the low power of LO signal, biased mixer approach was also considered to increase the multiplier sensitivity and to lower the output impedance. However, the biased mixer tested with the 2-element prototype exhibited sensitivity comparable with the non-biased ones. Therefore this approach was halted due to the additional complexity of the bias circuitry. During the operation, correlator modules were over-driven into the compression regime to ensure the noise contribution from the back-end electronics is a small percentage of that from receivers.

Although the output of an ideal double-balanced mixer is proportional to $V_{RF} \sinh(\alpha V_{LO})$ [7], a small amount of DC offsets were observed, possibly due to non-ideal behavior of baluns over the wide IF band or the cross talks between two inputs. They would saturate the subsequent DC amplifiers and readout circuits. Since the DC offsets don't change sign with respect to the phase switching, they can be removed by the high-pass filters at the inputs of DC amplifiers and the demodulation process.
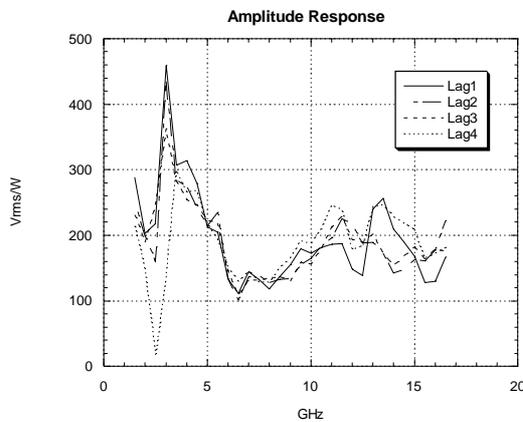
Fig. 5. Amplitude responses of a correlator module.   Fig. 6. Relative phase responses with respect to the 3rd lag.
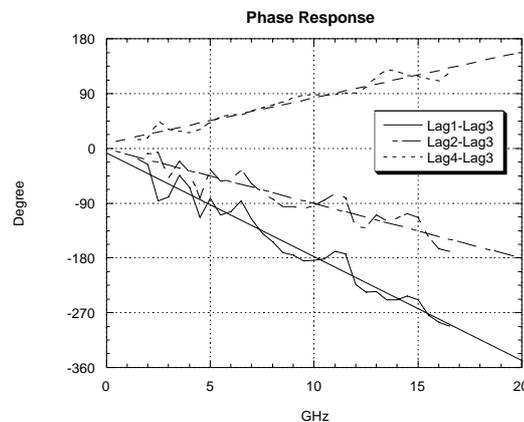
To characterize the correlator modules, two CW signals at frequencies of ω and $\omega+\delta\omega$ were fed into the correlator module. The low frequency output of i-th multiplier can be described as $A_i(\omega)v_1 v_2 \cos(\delta\omega t + \omega\tau_i + \phi_i(\omega))$ if amplitude variation $A(\omega)$ and phase error $\phi(\omega)$ in the passband are considered. The outputs were detected with a lock-in amplifier using one of outputs as the reference. As the frequency was swept across the IF band, the amplitude

and relative phase responses, namely, $A_i(\omega)$ and $\omega(\tau_i - \tau_j) + \phi_i(\omega) - \phi_j(\omega)$, were recorded. For amplitude response (Fig. 5), the results showed a broad hump of a peak value greater than 400 V_{rms}/Watt around 3 GHz, and above 100 V_{rms}/Watt for the remaining IF band. The relative phase responses (Fig. 6) were fitted linearly to find out the slopes, which correspond to delay differences between lags. The phase errors (the amount that deviated from the linear fitting) are within +/- 45 degrees. Dispersion is not seen at higher frequencies.
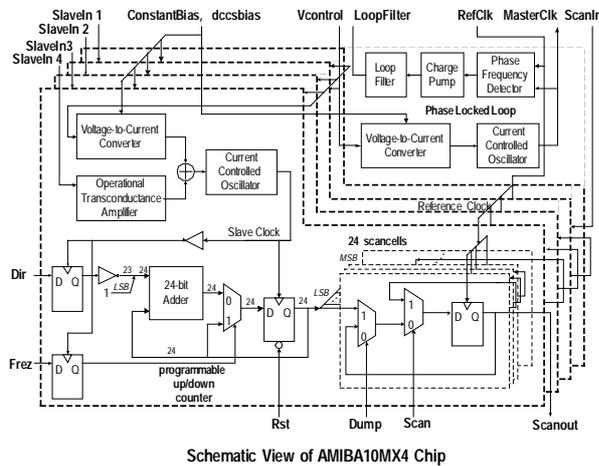
Fig. 7. Schematic of the back-end processing IC
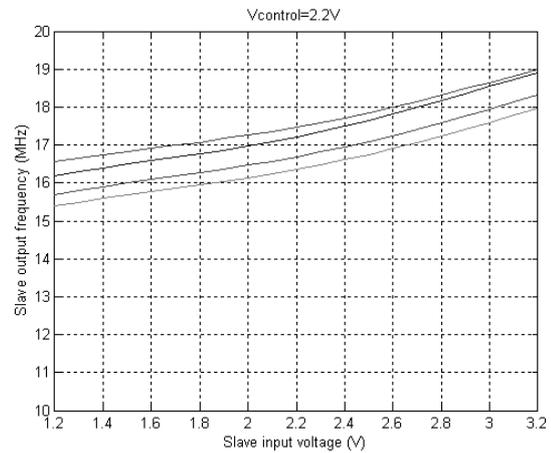
Fig. 8. Oscillation frequencies of slave VCOs as a function of input voltages with Vcontrol = 2.2V

5. BACKEND PROCESSING IC

The correlator backend processing IC[8] transforms the analog signals from the lag-correlator multipliers into digital pulse sequences and accumulates them with up/down counters, which acts as a long-term integrator plus phase-switching demodulator. The IC consists of a master phase locked loop (PLL) slave voltage-controlled oscillator (VCO) structure:

1. The PLL in the master circuit can be used to adjust the control voltage of a master VCO (by connecting LoopFilter and Vcontrol in Fig. 7) in order to generate a pulsing signal that is synchronized to the reference clock.
2. Four slave VCOs can be biased at either a constant voltage or the adjusted control voltage from PLL. An input analog signal is also incorporated in the bias voltage of each VCO and the VCO output frequency will scales almost linearly with the respective input. As shown in Fig. 8, when Vcontrol is anchored to 2.2V, the oscillation frequencies of slave VCOs vary between 15 to 19 MHz for the nominal (1.2 – 3.2 V) slave VCO input range. The increase in oscillation frequency (by increasing Vcontrol) can reduce the quantization noise to improve signal-to-noise ratio.

The four slave VCO outputs are used to trigger four 24-bit up/down counters to accumulate the digital data. The up/down function is controlled by the demodulation signal. At the end of an integration interval, the contents of the counters are scanned out serially.

6. SPECTRUM RECOVERY

For calibration, a W-band noise source was mounted on a carriage translating at a constant speed along the baseline of the 2-element prototype to vary the delay to each receiver. 2 reflectors were removed temporarily, and the coherent noise signals were coupled to the feedhorns through two 45-degree mirrors. The inteferometric outcomes of correlator modules – the fringes – were recorded, as shown in Fig. 9. By discrete Fourier transforming the fringe data $F(\tau)$ with respect to delay τ, the cross spectrum $W(f)$ of each lag can be derived as

$$W_m(f_n) = \sum_j F_m(\tau_j) \exp(i\, 2\pi f_n \tau_j) \Delta\tau \,, \tag{1}$$

where τ_j is the nominal delay difference presented to two inputs of each multiplier. As the noise source has a uniform power spectrum, the spectra reflect the passband properties of each lag, both amplitude and phase, as shown in Fig. 10. With delay range of about 660 pico-seconds, the current frequency resolution is set around 1.6 GHz. The spectral structures were dominated by correlator modules.

By Fourier transforming the fringe with the effect of a constant delay removed, namely,

$$W_m'(f_n) = \sum_j F_m(\tau_j) \exp(-i\, 2\pi f_n (\tau_j - \tau_{m\_0})) \Delta\tau \,, \tag{2}$$

where τ_{m_0} is chosen to be when the peak of each fringe is, the effective bandwidth can be estimated as[9]

$$BW_{effective\_m} = \left| \sum_n W_m'(f_n)\, \Delta f \right|^2 \Bigg/ \sum_n \left| W_m'(f_n) \right|^2 \Delta f \,. \tag{3}$$

The effective bandwidths were estimated to be around 13 GHz. At present, the amplitude response of lower band is about 3dB better than the higher band, indicating the effective bandwidth could be further improved using 3-dB slope equalizers.

With hot/cold load experiments, the additional noise temperature that the noise source presents to the receivers was calibrated to be about 27K. By comparing the signal strength of fringe and the output fluctuation without signal input, the signal to noise (S/N) ratio is determined. The system sensitivity with a 0.2 second integration time for each data point was determined to be on the order of few mK.

Since the correlated output of the mth lag can be written as

$$r_m = \sum_n A_{n,m} v_{1n} v_{2n} \cos(2\pi f_n (\tau_m + \tau) + \phi_1 - \phi_2 + \phi_{n,m}) \,, \tag{4}$$

where $A_{n,m}$ the amplitude response variation, τ_m the built-in delay for m[th] lag, and $\phi_{n,m}$ the phase error. With matrix notation,

$$sK$$

$$= \begin{bmatrix} s_{-N} & \cdots & s_{-2} & s_{-1} & s_1 & s_2 & \cdots & s_n & \cdots & s_N \end{bmatrix}
\begin{bmatrix}
K_{-N,1} & \cdots & \cdots & K_{-N,M} \\
\vdots & & & \\
K_{-2,1} & & K_{-n,m} & \\
K_{-1,1} & & & \\
K_{1,1} & K_{1,2} & \cdots & K_{1,M} \\
K_{2,1} & & & \\
\vdots & & & \\
K_{n,1} & & K_{n,m} & \\
\vdots & & & \vdots \\
K_{N,1} & \cdots & \cdots & K_{N,M}
\end{bmatrix} \,, \tag{5}$$

$$= r$$

$$= \begin{bmatrix} r_1 & r_2 & \cdots & r_m & \cdots & r_M \end{bmatrix}$$

where the element of the transform matrix $K_{\pm n,m} = A_{n,m} \exp(\pm i (2\pi f_n \tau_m + \phi_{n,m}))$, and cross spectrum element

$$s_{\pm n} = \frac{v_{1n} v_{2n}}{2} \exp(\pm i (2\pi f_n \tau + \phi_1 - \phi_2)) \,.$$

The passband properties $W_m(f_n)$ can be substituted for the matrix element $K_{n,m}$. Hereafter, the inverse of the transform matrix K can be applied to the fringe to obtain the cross spectrum of incoming signals. Since the frequency resolution obtained is finer than that given by 4-lag correlators, the transformation matrix K would be singular if it were not for measurement noise or non-ideal phase/amplitude responses of each multiplier. Owing to the nearly singular matrix, singular value decomposition[10] (SVD) is used to invert K. A routine ZGESVD in LAPACK is applied to the complex matrix. The final spectra were averaged into two bins to reflect the actual frequency resolution, as shown in Fig. 11 for data around the phase center of the 2-element system. In the final operation, as a point source drifts past the interferometer, the smaller delay range, set by the primary beam pattern, would yield the frequency resolution close to that given by 4-lag correlators.

7. CONCLUSION

A wideband correlation system for AMiBA with 13 elements has been designed and implemented. The effective bandwidth achieved thus far is around 13 GHz. By adjusting the gain profile, further improvement is feasible. A preliminary calibration and spectrum recovery method has been illustrated with the data from the 2-element prototype.

ACKNOWLEDGEMENTS

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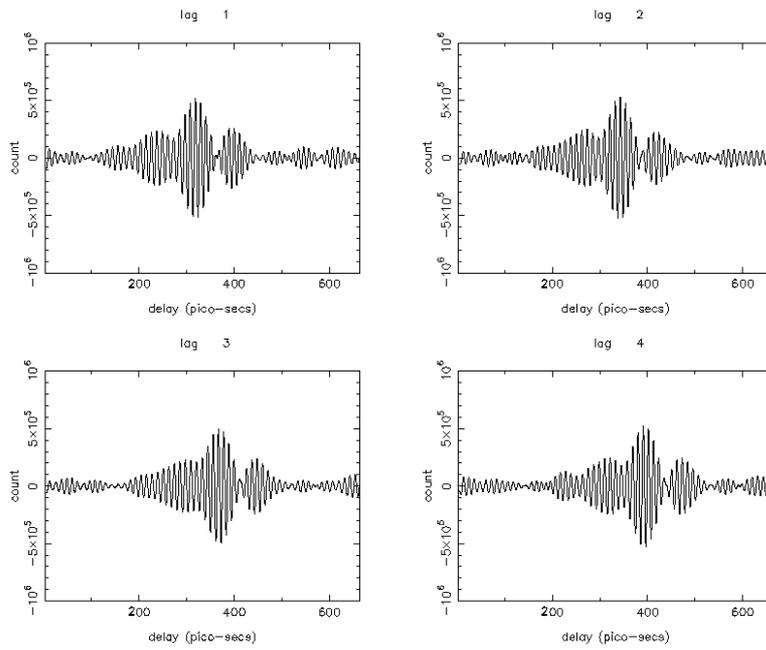
Fig. 9. The fringe recorded with a translating noise source.
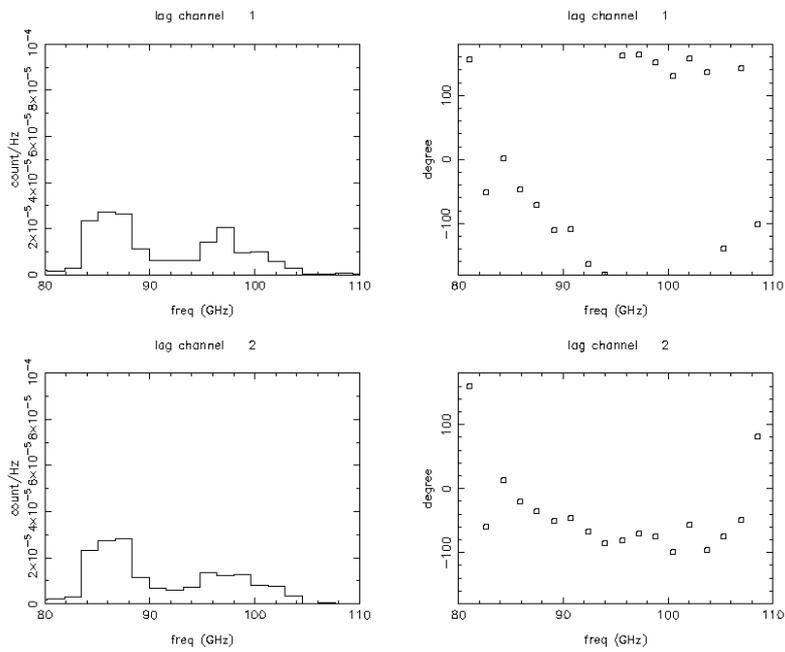
Fig. 10.a.   Cross power spectra of each lag transformed from the fringe data.
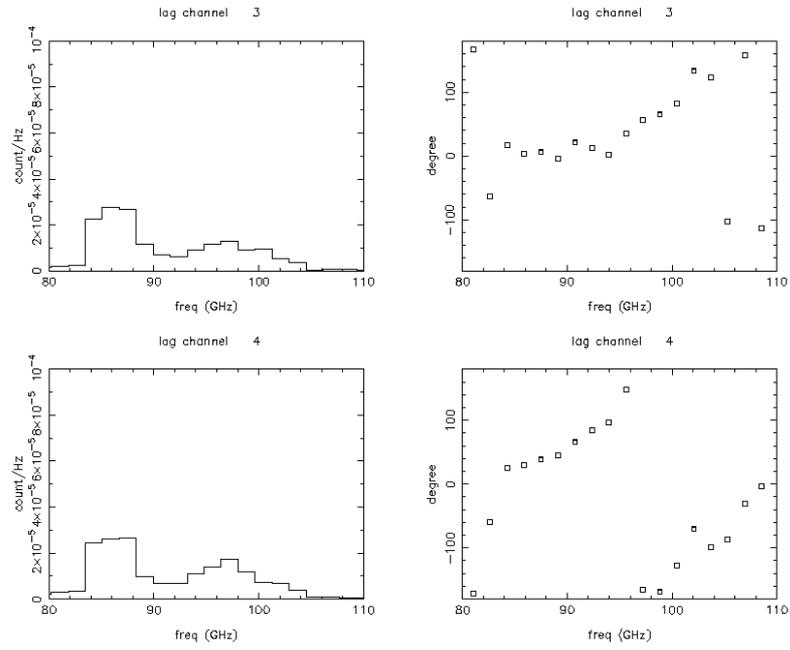
Fig. 10.b.   Cross power spectra of each lag transformed from the fringe data.
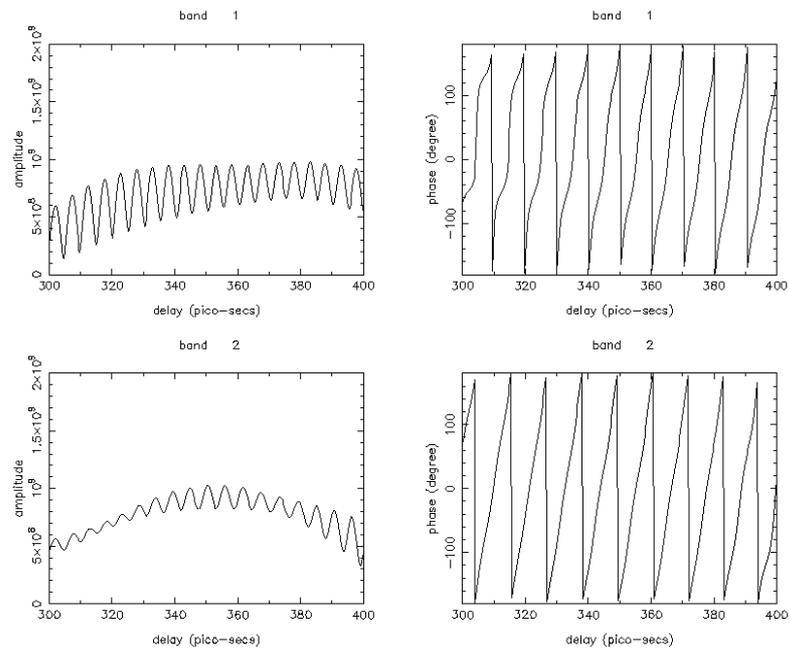
Fig. 11. Input power spectra in two bands - band 1 (84-94 GHz), band 2 (94-104 GHz) - as the inverse matrix was applied to the fringe data.