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Event: SPIE Astronomical Telescopes + Instrumentation, 2022, Montréal, Québec, Canada

## wSMA superconducting diplexer development

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#### ABSTRACT

Diplexers were developed to separate a wide intermediate frequency (IF) range and utilize IF below 4 GHz for wideband submillimeter array (wSMA) receivers. Diplexers were designed using superconducting materials and processed via inhouse thin film fabrication. The diplexers were designed to operate around 4 K and can be integrated with other cryogenic components.

Keywords: diplexer, superconducting circuit, wideband submillimeter array

#### I. INTRODUCTION

In astronomical observations, wider bandwidths can enable the gathering of more information (e.g., more spectral lines or samples). Initially, submillimeter array receivers used 4–6 GHz as the intermediate frequency (IF), which was later increased to 4–14 GHz [1]. To further expand it, moving toward higher IFs, such 20 GHz, is an option; another approach is to exploit IFs below 4 GHz. The latter option would allow almost continual RF sampling below and above the LO frequency.

A diplexer is employed when frequency multiplexing is required, such as a transceiver that transmits and receives signals in different frequency bands via the same antenna. Diplexers can have various configurations, such as lowpass/highpass or bandpass/bandpass. We selected a lowpass/highpass scheme because of the large fractional bandwidths (0.1-4 GHz and 4-16+ GHz) we are dealing with. We designed diplexers to separate IF from dc to 16 GHz at 4 GHz for subsequent amplification and processing, as shown in Fig. 1.

Photolithography can be used to develop features with micron scale accuracy, which is considerably more accurate than printed circuit board manufacturing. Thus, photolithography enables the fabrication of transmission lines with large impedance ratios. However, high-impedance transmission lines are typically narrow and lossy. Superconducting films can help reduce the losses of such transmission lines.



Fig. 1. Schematic of wSMA receiver with a diplexer.

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Millimeter, Submillimeter, and Far-Infrared Detectors and Instrumentation for Astronomy XI, edited by Jonas Zmuidzinas, Jian-Rong Gao, Proc. of SPIE Vol. 12190, 121901H · © 2022 SPIE · 0277-786X · doi: 10.1117/12.2628429

#### II. DESIGN

Lowpass and highpass filters were designed first. Periodic structures were adopted for the first lowpass filter design. A high stepped impedance ratio scheme was used in the second design iteration. For the highpass filter, one inductor/capacitor (LC) stage was used. The lowpass and highpass filters were then combined to form the diplexer.

#### A. Lowpass Filter

A periodic structure comprising uniform transmission line sections can be used to construct a lowpass filter [2]. The responses of each unit cell, such as passband and stopband, can be analyzed in terms of the dispersion relationship. Techniques described in [3], such as setting  $A_s = D$  and employing two-section transmission lines to mimic ideal T junctions, can suppress an undesired passband and merge two adjacent stopbands to create a wider stopband. Following the two Cell C filter design [3], we designed the lowpass filter with an  $f_{cl}$  of approximately 3.5 GHz and relative stop bandwidth (RSB) of approximately 133%.

Our circuit was designed based on a 450-nm-thick Nb film deposited on a 0.25-mm-thick fused quartz substrate (relative dielectric  $\varepsilon_r$  of approximately 3.8). The high impedance of the uniform transmission line Z was set to 109  $\Omega$ , with  $Z_s = 31.8$   $\Omega$ . The schematic and simulated responses of the lowpass filter with two cascaded unit cells are shown in Fig. 2. The dimensions of one unit cell are shown in Fig. 3.



Fig. 2. [Top] Schematic of two cascaded unit cells; [Bottom] simulated responses of the lowpass filter (green: transmission; red: reflection).



Fig. 3. Dimensions (in mm) of unit cell of the lowpass filter

#### B. Highpass Filter

For the highpass filter, a series capacitor with a shunt inductor was used, as shown in Fig. 4. The inductor was made of a narrow high-impedance transmission line. In the first design iteration, a parallel-plate capacitor comprising two overlapping electrodes with a dielectric (250-nm SiO<sub>x</sub>,  $\varepsilon_r$  of approximately 4) in between was used. The capacitance can be estimated as follows:

$$C = \varepsilon_r \varepsilon_0 A/d,\tag{1}$$

where A is the overlapping area and d is the thickness of the dielectric material. An electromagnetic (EM) model of the highpass filter and the simulation results with a 3D EM simulator (HFSS) [4] are shown in Fig. 5.



Fig. 4. Schematic of the highpass filter.





Fig. 5. [Top] EM model and [Bottom] simulated results (purple: transmission; red: reflection) of the highpass filter. Highimpedance line acts as an inductor to the ground.

In the second design iteration, we used interdigital capacitors because they are easier to fabricate. An EM model of the interdigital capacitor and the simulated responses are shown in Fig. 6. The transmission of a serial capacitor can be expressed as follows [2]:

$$S_{21} = \frac{j_{2\omega CZ_0}}{1 + j_{2\omega CZ_0}},$$
(2)

The capacitance was extracted to be approximately 0.43 pF.



Fig. 6. [Left] EM model of the interdigital capacitor. Each finger is 10 µm wide and 215 µm long with 5 µm gap. [Right] Simulated transmission (red) and reflection (purple) were fitted to extract the capacitance.

#### C. Diplexer

The circuits of lowpass and highpass filters were combined and the circuit of the diplexer, shown in Fig. 7, was optimized; the design was then ported to the 3D EM simulator. A 3D model of the diplexer with an interdigital capacitor and the simulation results are shown in Fig. 8.



Fig. 7. Circuit schematic of the diplexer.



Fig. 8. [Top] EM model of the diplexer with interdigital capacitor. [Bottom] Simulation results (blue: lowpass transmission; red: lowpass reflection; purple: highpass transmission; green: highpass reflection).

### III. FABRICATION AND TESTING

The diplexer was fabricated on a 250- $\mu$ m-thick fused quartz substrate with  $\epsilon_r$  of approximately 3.8. The circuit comprised an approximately 450-nm-thick Nb film with a layer of approximately 200-nm-thick Au on top for contact. For the design

with a parallel-plate capacitor, the bottom and top electrodes were 150 nm and 300 nm thick, respectively; the dielectric between the electrodes was 250-nm-thick  $SiO_x$  with an  $\varepsilon_r$  of approximately 4. The fabricated device is shown in Fig. 9. The device with the interdigital capacitor was also fabricated and is shown in Fig. 10.



Fig. 9. Diplexer with parallel-plate capacitor.





The device was mounted into a housing with 50- $\Omega$  microstrip transmission lines [5] placed between the diplexer and connectors. 1-mil gold wires were bonded between components, as shown in Fig. 11. Subsequently, the module was loaded into a cryostat and tested with a vector network analyzer at room temperature and around 4 K, as shown in Fig. 12. The room temperature measurements and the simulation results with the circuit set to be a perfect conductor are plotted in Fig. 13. The transmission measurements are consistent with the simulation results, except for the conductor loss. Transmission measurements were also performed at approximately 5 K; in this case, the passband transmission loss decreased because the Nb film became superconducting. However, the device response shifted to higher frequencies when it was cooled. Once we adopted the surface impedance of the superconducting film as follows [6]:

$$Z_s = j\omega\mu_0\lambda_L \coth(t/\lambda_L) \tag{3}$$

where t is the film thickness and the London penetration depth  $\lambda_L$  of the Nb film was set to 0.1 µm, the measurements agree well with the simulation results, as shown in Fig. 14.



Fig. 11. [Left] Diplexer packaged in a housing; [Right] bonding wires between components.



Fig. 12. [Left] Diplexer mounted into a 4 K cryostat and [Right] tested using a vector network analyzer.





Fig. 13. [Upper] Transmission measurements of diplexer at room temperature and simulation results with the circuit set to be a perfect conductor; [Lower] tested around 5 K.



Fig. 14. Measurements of diplexer around 5 K, together with simulation results when the surface impedance of the superconducting film was used.

#### **IV. MINIATURIZATION**

For a stepped-impedance lowpass filter, a high impedance ratio is the key to wideband cutoff. In addition, the circuit can be miniaturized to some extent for integration with other components, like superconductor–insulator–superconductor (SIS) mixers, bias circuitry, and cryogenic low noise amplifiers. Using thin film fabrication techniques, transmission lines with impedances as high as 196  $\Omega$  or down to 2  $\Omega$  can be realized. A lowpass filter based on this high stepped impedance ratio was designed, as shown in Fig. 15. After the highpass filter was incorporated, the dimensions of the diplexer were further reduced using some meandering lines, as shown in Fig. 16.



Fig. 15. [Top] Schematic of stepped-impedance lowpass filter with a high impedance ratio; [Bottom] simulation results (green: transmission; red: reflection).





Fig. 16. [Top] EM model of diplexer with high-stepped impedance ratio lowpass filter; [Bottom] simulation results (green: lowpass transmission; red: lowpass reflection; orange: highpass transmission; blue: highpass reflection).

#### V. DISCUSSION

The measurement results agree well with the EM simulations if the surface impedance of superconducting films is taken into account. Some transmission dips occurring at high frequencies might be due to packaging effects. Distance to fault (DTF) measurements indicated that significant reflections occur around bonding wires. Various packaging approaches will be investigated to mitigate this problem. Furthermore a miniaturized diplexer incorporating a high–stepped impedance ratio lowpass filter was designed for system integration consideration.

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